

<b>Notice of References Cited</b>	Application/Control No. 10/616,647		Applicant(s)/Patent Under Reexamination HUANG ET AL.	
	Examiner BENJAMIN P. GEIB		Art Unit 2181	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,430,851	07-1995	Hirata et al.	712/212
*	B	US-5,913,049	06-1999	Shiell et al.	712/215
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Hirata et al.; "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads"; 1992; ACM			
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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